

THAT WHICH IS CLAIMED IS:

1. An integrated circuit chip comprising:
a search engine including a content addressable memory (CAM) configured to produce CAM indices responsive to search instructions provided to the search engine and an index translation circuit operatively coupled to the CAM and configured to provide translation of the CAM indices.
2. A chip according to Claim 1, wherein the index translation circuit is configurable to provide independent index mappings for respective segments of the CAM.
3. A chip according to Claim 1, wherein the index translation circuit is configured to receive CAM indices from a second search engine device and is configurable to provide independent index mappings for respective segments of the second search machine device.
4. A chip according to Claim 1, wherein the index translation circuit is configurable to provide independent index mappings for respective databases.
5. A chip according to Claim 1, wherein the index translation circuit is configurable to provide translation of the CAM indices to any of a plurality of memory spaces.
6. A chip according to Claim 5, wherein the index translation circuit is configurable to provide translation of absolute indices associated with a search machine comprising the search engine to database relative indices and memory addresses.

7. A chip according to Claim 6, wherein the memory addresses are memory addresses in a memory space associated with a command source for the search engine.

8. A chip according to Claim 6, wherein the memory addresses are memory addresses in a memory space of a memory device external to the chip.

9. A chip according to Claim 8, wherein the memory interface circuit comprises a static random access memory (SRAM) interface.

10. A chip according to Claim 8, wherein the index translation circuit is configurable to provide compaction of the memory space of the external memory device.

11. A chip according to Claim 1, wherein the index translation circuit comprises a mapping table operative to associate respective combinations of a shift factor and a base address for a database with respective CAM segment identifiers, wherein the shift factors indicate database entry size, and wherein the index translation circuit is operative to receive a CAM index, to identify a base address and a shift factor corresponding to a CAM segment identifier in the received CAM index, to concatenate the identified base address with a segment entry offset in the received CAM index, and to shift the concatenated result according to the identified shift factor to produce a database relative index corresponding to the received CAM index.

12. A chip according to Claim 1, wherein the index translation circuit comprises a mapping table operative to associate respective combinations of a shift factor and a base address for a memory space external to the chip with respective CAM segment identifiers, wherein the

shift factors indicate a data size in the memory space and an entry size of CAM space corresponding to the memory space, and wherein the index translation circuit is operative receive a CAM index, to identify a shift factor and a base address corresponding to a CAM segment identifier in the received CAM index, to shift a segment entry offset in the received CAM index according to the identified shift factor, and to add the shifted result to the identified base address to produce a memory address in the external memory space corresponding to the received CAM index.

13. An integrated circuit chip comprising:

a search engine including a content addressable memory (CAM) configurable to store a plurality of databases and operative to produce CAM indices in an index space of a search machine comprising the search engine responsive to search instructions provided to the search engine and an index translation circuit operatively coupled to the CAM and configured to translate the CAM indices produced by the CAM to database relative indices.

14. A chip according to Claim 13, wherein the index translation circuit is configurable to provide independent index mappings for respective segments of the CAM.

15. A chip according to Claim 14, wherein the index translation circuit is configured to receive CAM indices from a second search machine device and is configurable to provide independent CAM index mappings for respective segments of the second search machine device.

16. A chip according to Claim 13, wherein the index translation circuit is configured to receive CAM indices from a second search machine device and operative to translate the received CAM indices to database relative indices.

17. A chip according to Claim 13, wherein the index translation circuit is further configurable to translate CAM indices to memory addresses.

18. A chip according to Claim 17, wherein the index translation circuit is configurable to provide database relative indices or memory addresses on a segment-by-segment basis.

19. A chip according to Claim 17, wherein the index translation circuit is configurable to translate CAM indices to memory addresses associated with a search command source and/or memory addresses associated with an external memory.

20. A chip according to Claim 19, wherein the index translation circuit is operative to provide compaction of the address space of the external memory.

21. A chip according to Claim 13, wherein the index translation circuit comprises a mapping table operative to associate respective combinations of a shift factor and a base address for a database with respective CAM segment identifiers, wherein the shift factors indicate database entry size, and wherein the index translation circuit is operative to receive a CAM index, to identify a base address and a shift factor corresponding to a CAM segment identifier in the received CAM index, to concatenate the identified base address with a segment entry offset in the received CAM index, and to shift the concatenated result according to the identified shift factor to produce a database relative index corresponding to the received CAM index.

22. A chip according to Claim 13, wherein the index translation circuit comprises a mapping table operative to associate respective

combinations of a shift factor and a base address for a memory space external to the chip with respective CAM segment identifiers, wherein the shift factors indicate a data size in the memory space and an entry size of CAM space corresponding to the memory space, and wherein the index translation circuit is operative receive a CAM index, to identify a shift factor and a base address corresponding to a CAM segment identifier in the received CAM index, to shift a segment entry offset in the received CAM index according to the identified shift factor, and to add the shifted result to the identified base address to produce a memory address in the external memory space corresponding to the received CAM index.

23. An integrated circuit chip comprising:

a search engine including a content addressable memory (CAM) and a programmable index translation circuit operatively coupled to the CAM and configurable to provide a plurality of different index translations.

24. A chip according to Claim 23, wherein the index translation circuit comprises a programmable mapping table configurable to provide a plurality of index translations.

25. A chip according to Claim 24, wherein the mapping table is configurable to map indices to database relative indices and/or memory addresses for a memory space external to the chip.

26. A chip according to Claim 24, wherein the mapping table is configurable to provide respective index mappings for respective CAM segments.

27. A chip according to Claim 24, wherein the mapping table is configurable to provide respective index mappings for respective databases.

28. A chip according to Claim 24, wherein the mapping table is configurable to associate respective combinations of a shift factor and a base address for a database with respective CAM segment identifiers, wherein the shift factors indicate database entry size, and wherein the index translation circuit is operative to receive a CAM index, to identify a base address and a shift factor corresponding to a CAM segment identifier in the received CAM index, to concatenate the identified base address with a segment entry offset in the received CAM index, and to shift the concatenated result according to the identified shift factor to produce a database relative index corresponding to the received CAM index.

29. A chip according to Claim 24, wherein the mapping table is configurable to associate respective combinations of a shift factor and a base address for a memory space external to the chip with respective CAM segment identifiers, wherein the shift factors indicate a data size in the memory space and an entry size of CAM space corresponding to the memory space, and wherein the index translation circuit is operative receive a CAM index, to identify a shift factor and a base address corresponding to a CAM segment identifier in the received CAM index, to shift a segment entry offset in the received CAM index according to the identified shift factor, and to add the shifted result to the identified base address to produce a memory address in the external memory space corresponding to the received CAM index.

30. An integrated circuit chip comprising:
a search engine comprising a content addressable memory (CAM) configured to produce CAM indices responsive to search instructions provided to the search engine and an index translation circuit operatively coupled to the CAM and configured to store memory entry size information and to provide translation of the CAM indices to another memory space based on the stored memory entry size information.

31. A chip according to Claim 30, wherein the memory entry size information comprises entry size information for a database in the CAM.

32. A chip according to Claim 30, wherein the memory entry size information comprises entry size information for a memory external to the chip.

33. A chip according to Claim 30, wherein the index translation circuit is configured to store a base address for a memory space and a shift factor indicating a data entry size for the memory space and to generate a translated address or index from a CAM index according to the base address and the shift factor.

34. A chip according to Claim 33, wherein the memory space comprises one of a database, a memory space associated with a command source for the search engine, and a memory space of a external memory device.

35. A chip according to Claim 33, wherein the shift factor further indicates a data entry size for the CAM.

36. An integrated circuit chip comprising:
a search engine comprising a content addressable memory (CAM)

comprising a plurality of segments and configured to produce CAM indices responsive to search instructions provided to the search engine and an index translation circuit operatively coupled to the CAM and configurable to map CAM indices for selected ones of the CAM segments to addresses in a memory space external to the chip.

37. A chip according to Claim 36, wherein the index translation circuit is operative to provide compact data storage of data corresponding to the CAM indices in the external memory.

38. A method of operating a search machine comprising at least one integrated circuit search engine chip, the method comprising:

providing a search instruction to the search machine;

generating a content addressable memory (CAM) index in an absolute index domain comprising a searchable memory space of the search machine responsive to the search instruction;

translating the CAM index to a second memory space to produce a translated index; and

providing the translated index to a device external to the search machine.

39. A method according to Claim 38, wherein the second memory space comprises one of a database, a memory space associated with a command source for the search machine, and a memory source addressable by the search machine.

40. A method according to Claim 38, further comprising configuring a segment mapping table in the at least one search engine chip to provide translation of absolute indices to at least one of database relative indices, command source memory pointers and search engine associated external memory addresses.

41. A method according to Claim 38, wherein configuring a segment mapping table comprises providing respective index translations for respective segments of the search machine.